Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **1A**
2. **1B**
3. **1Y**
4. **2A**
5. **2B**
6. **2Y**
7. **GND**
8. **3Y**
9. **3A**
10. **3B**
11. **4Y**
12. **4A**
13. **4B**
14. **VCC**

**.032”**

**.037”**

**12 11 10 9**

**2 3 4 5**

**13**

**14**

**1**

**8**

**7**

**6**

**L**

**S**

**0**

**0**

**C**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size: .0034” X .0034”**

**Backside Potential: GND**

**Mask Ref: LS00C**

**APPROVED BY: DK DIE SIZE .032” X .037” DATE: 8/30/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .024” P/N: 54LS00**

**DG 10.1.2**

#### Rev B, 7/19/02